REMARKS

Request for Continued Examination

Applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

Claims 1, 3-4 and 9-11 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Ahn (USPN: 6,564,283) in view of Kaneko (USPN: 5,146,581)

Claims 1, 3-4 and 9-11 are cancelled.

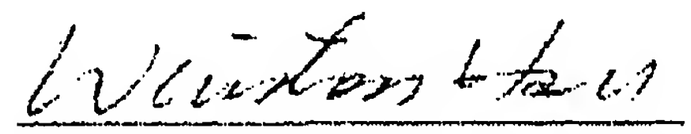
New Claims

New claims 15-28 are added. No new matter is entered. In particular, new independent claims 15 and 22 are disclosed in Fig.4 and the associated paragraphs [19], [20], and [25] of the present invention. In particular, paragraph [25] states, "... the common areas of all pages are mapped onto a single physical region of the external memory". Dependent claims 16 and 23 are disclosed in Fig.2 and the description of paragraph [8] stating, "Because the common area data is duplicated at the same relative location in each page, the MCS microprocessor 1 is able to access the common data regardless of the state of pins P1.0-2." Also note that the address translator 24 of Fig.6 generates the select signal 49 according to the same comparison of addresses A regardless of which page (P1.0-P1.3) is selected. Dependent claims 17 and 24 are disclosed in paragraph [20] stating, "whenever the MCS microprocessor accesses an address not belonging to the common area, the address translator converts the logical address to the physical address inside the non-common area of the external memory." Dependent claims 18, 19, 25 and 26 are shown in Fig.5 having a plurality of non-common areas (Page 0 – 9) and disclosed in paragraph [20] stating, "P is the translated physical address to the external memory, and N and A are the logical page

index and address of the data that is being accessed by the MCS microprocessor." Dependent claims 20 and 27 are disclosed in Fig.6 and paragraphs [21] and [22]. Finally, dependent claims 21 and 28 are disclosed in paragraph [23] stating, "the content of the common area size bus 43 can be provided by programmable registers rather than being fixed at a constant value".

Concerning the patentability of new independent claims 15 and 22 with respect to the cited references of Ahn and Kaneko, applicant points out that neither Ahn nor Kaneko teach, "mapping a predetermined range of addresses within all pages pointed to by the microprocessor when accessing the external memory into the single physical region of the external memory", as is claimed in claims 15 and 22. For at least this reason, applicant asserts that claims 15 and 22 should be found allowable with respect to the teachings of Ahn and Kaneko. As claims 16-21 and 23-28 are dependent on claims 15 and 22, respectively, if claims 15 and 22 are found allowable, so too should the dependent claims 16-21 and 23-28 for at least the same reasons. Consideration of new claims 15-28 is respectfully requested.

Sincerely yours,



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